# उच्च तीव्रता प्रोटॉन त्वरक

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# आईआईएफसी के तहत त्वरकों के लिए एकीकृत आरएफ नियंत्रण प्रणाली का विकास

निबंध कुमार, राधिका नासेरी, आलोक आगाशे, सुजो सी.आई., संदीप भराडे, आर. टी. केशवानी, सुरेंद्र सिंह सैनी, जी. रंदाले, पी. ज्योथि, परेश मोतीवाला और *गोपाल जोशी

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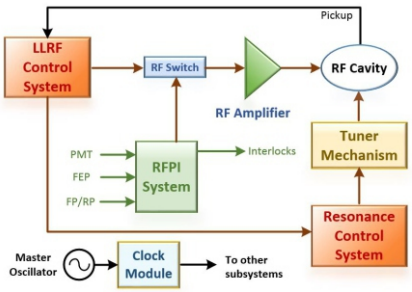


*एकीकृत आरएफ नियंत्रण प्रणाली*

सारांश

भारतीय संस्थानों और फर्मीलैब सहयोग के अंतर्गत त्वरक के लिए विकसित एकीकृत रेडियो आवृत्ति नियंत्रण प्रणाली गुहाओं के अंदर रेडियो आवृत्ति क्षेत्र के आयाम और चरण को नियंत्रित करने, रेडियो आवृत्ति गुहाओं की अनुनाद आवृत्ति की निगरानी करने, स्टेपर मोटर्स और पीजो एक्चुएटर का उपयोग करके गुहा अनुनाद आवृत्ति को बनाए रखने, त्वरक में महत्वपूर्ण आर. एफ. घटकों की सुरक्षा, और सभी उप प्रणालियों के समन्वय के लिए सटीक समय प्रदान करने के महत्वपूर्ण कार्य करती हैं। त्वरित गुहिका में रेडियो आवृत्ति क्षेत्र की स्थिरता आवेशित कणों की प्रभावी त्वरितता और कणपुंज के ऊर्जा प्रसार को कम बनाए रखने के लिए अत्यंत महत्वपूर्ण है। उच्च शक्ति वाले रेडियो आवृत्ति घटकों जैसे रेडियो आवृत्ति खिड़कियाँ, युग्मक, रेडियो आवृत्ति शक्ति स्रोत, तरंग मार्गदर्शिका, रेडियो आवृत्ति गुहा आदि की सुरक्षा के लिए रेडियो आवृत्ति सुरक्षा और इंटरलॉक (आर. एफ. पी. आई.) प्रणाली का उपयोग किया जाता है। एक एकीकृत रेडियो आवृत्ति नियंत्रण प्रणाली, जिसमें निम्न स्तरीय रेडियो आवृत्ति नियंत्रण प्रणाली, अनुनाद नियंत्रण प्रणाली , और रेडियो आवृत्ति संरक्षण और अंतरबंध प्रणाली शामिल हैं, को RRCAT, इंदौर में 650 मेगाहट्र्ज अति चालक गुहा के परीक्षण के लिए स्थापित किया गया है।

# High Intensity Proton Accelerator

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# Integrated RF Control System Developed for Accelerators Under IIFC

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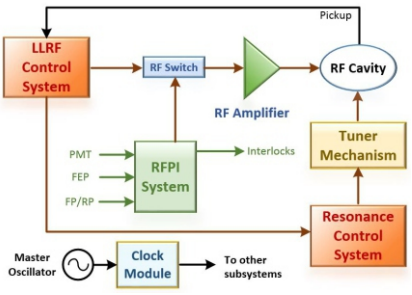


*Integrated RF Control System*

ABSTRACT

Integrated RF control system developed under Indian Institutions and Fermilab Collaboration (IIFC) performs important functions of controlling the amplitude & phase of the RF field inside the cavities, track the resonance frequency of RF cavities, maintain the cavity resonance frequency using stepper motors and piezo actuators, protection of critical RF components in the accelerator, and providing precision timing for synchronization to all the sub systems. Stabilization of RF field in an accelerating cavity is critical for efficient acceleration of the charged particles and maintaining low energy spread of the beam [1]. For the protection of high power RF components, such as, RF windows, Couplers, RF power sources, waveguide, RF cavity etc. RF Protection and Interlock (RFPI) system is employed. An integrated RF control system, which includes Low Level RF (LLRF) control system, Resonance Control System (RCS) and RF Protection & Interlock (RFPI) system, has been commissioned for testing of 650 MHz superconducting RF cavities in HTS at RRCAT, Indore.

KEYWORDS: *Low level RF control, RF protection, Integrated RF control, Resonance control.*

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## Introduction

Under IIFC, an integrated RF control system has been developed for 650 MHz superconducting RF cavity and the same is depicted in Fig.1. Sub-systems within the dashed rectangle constitute an integrated RF control system. The LLRF system employs frequency conversion to/from an intermediate frequency (IF) of 20 MHz, using down/up converters. The remaining signal processing is carried out in digital domain in a Digital Module.

Superconducting RF cavities, for which this system is designed, have a loaded quality factor of the order of $10^7$ and therefore, the cavity is liable to get detuned due to Lorentz force, microphonics, helium pressure variations, slow drifts etc. RCS keeps the superconducting RF cavity at resonance and compensates for the cavity detuning to minimize RF power requirement. This is accomplished through electro-mechanical tuners coupled to the cavity. Coarse and fine adjustments in the cavity frequency can be made through the use of stepper motors coupled to the mechanical tuner assembly and piezoelectric actuators attached to the cavity. The electronics system of RCS is part of RF control system. The demodulated RF pick-up, forward & reflected power signals are transported from the LLRF system to the RCS via a multi Gb serial link for calculating the cavity detuning.

RFPI system, described in detail in the newsletter article 'RF Protection Interlock and Monitoring System developed for accelerators', continuously monitors sensor outputs installed with high power RF components and status signals from various sub-systems. This system, upon detecting a fault condition, removes the RF input from the input of the high power RF amplifier, thereby protecting the high power RF components.

## LLRF System Description

RF pickup signal at 650 MHz is down converted to an IF of 20 MHz and digitized using non-IQ sampling scheme [6]. Subsequent processing is carried out in digital domain. The processed IF signals in digital domain, after passing through DACs, are up-converted to generate suitable drive for the cavity. This scheme requires additional hardware in the form of down and up converters and offers high precision. Implementation using FPGAs and communications grade ADCs and DACs enables sub-microsecond delay in the LLRF feedback loop thereby enabling wider control bandwidth.

The 8 channel down-converter translates RF pick up signal from the cavity to IF signal using low phase noise LO signal of 670MHz, RF mixer and suitable filters. Whereas using the same LO signal the 4 channel up-converter module up converts the processed baseband signal back to RF for feeding

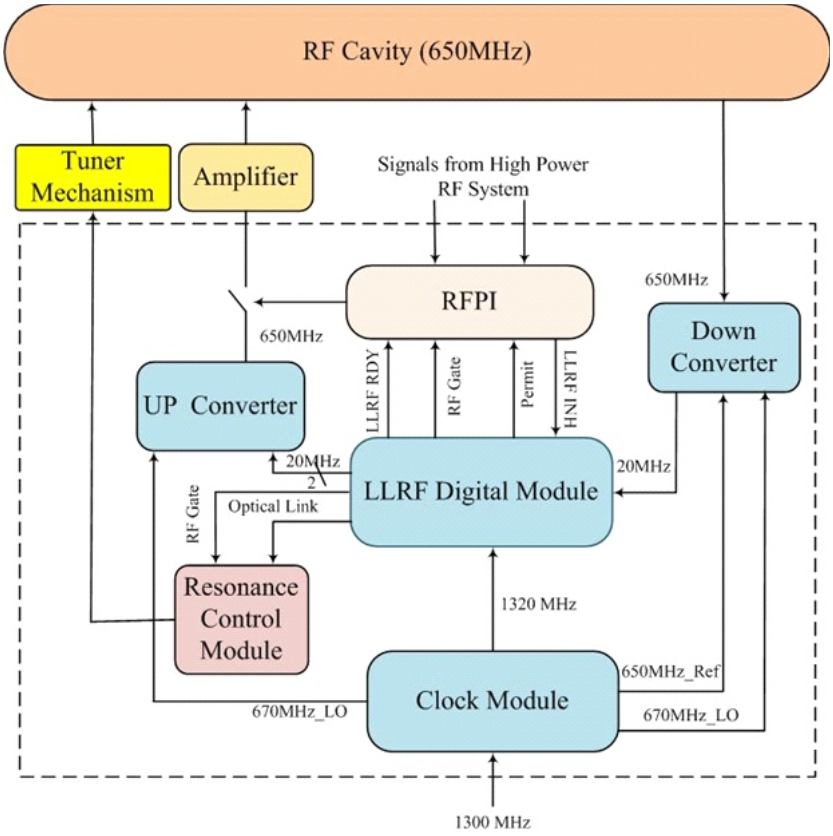


*Fig.1: Integrated RF Control System developed under IIFC.*


*Fig.2a: 8 channel down-converter and 4 Channel up-converter modules.*

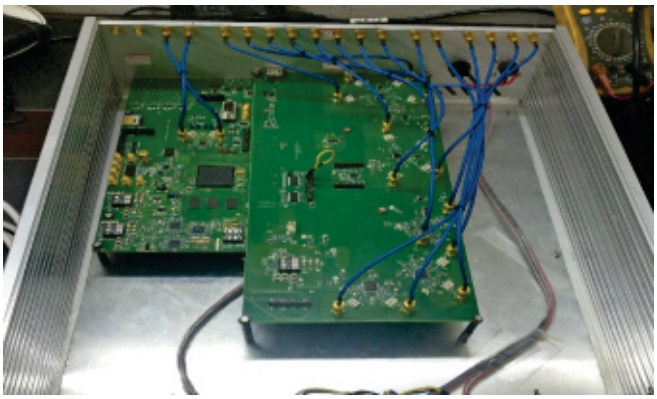

*Fig.2b:LLRF digital module.*

to the cavity after suitable amplification. Both the up and down converters (shown in Fig. 2a) designed to have high channel to channel to isolation (around 80dB) and linearity of better than 1% within the operating range. A high isolation (better than 60dB) RF switch has been provided at the output of each channel in the up-converter, which may be operated remotely to switch OFF the RF power to the cavity.

The Digital module, shown in Fig.2b, plays a key role in determining the overall targets of achieving high RF field stability of 0.01% in amplitude and 0.01 degrees in phase. The ADC in the Digital module is a high performance device with a 16-bit resolution and very low clock aperture jitter. The ADC sampling clock provides processing gain which helps improve the overall SNR of the system. High speed System on Chip (SoC) based FPGA situated in the digital module implements the entire digital signal processing chain. The FPGA provides interfaces such as Ethernet, USB, UART etc. to communicate with the host.

For achieving high precision, all the modules of the LLRF control system require stable and low phase noise RF sources. Generally, a Reference Phase Distribution System is provided in accelerator to meet this requirement. A separate article titled "Reference Phase Generation Systems Developed under IIFC" is included in this newsletter describing such a system in detail. For HTS this requirement is met by developing a Clock Module. The Clock Module accepts 1300MHz RF signal from a signal generator and generates all the necessary clocks for the LLRF system. Clock dividers with low additive phase noise, single side-band mixer circuits and cavity filters have been used for this purpose. The phase noise of LO signal at an offset frequency of 100 KHz is measured as -130 dBc/Hz.

## LLRF Digital Signal Chain Description

The digital signal processing chain is shown in Fig. 3. For each cavity, four signals viz; Cavity pick-up, RF Reference, Forward and Reflected are processed inside the FPGA for control and monitoring purposes. All the four incoming signals to FPGA are centred at an IF of 20MHz which is digitized with a 16 bit, quad channel Analog to digital converter. The demodulated pick-up signal is compared with the desired value. The resulting error signal is passed through a P-I controller to correct the errors. The output signals are digitally up converted to 20MHz and sent to DAC.

The firmware and software of LLRF system enables operation in Generator Driven Resonator (GDR), Self Excited Loop (SEL) and Open Loop modes of operation. In GDR mode the cavity is driven with RF signal, phase synchronized with the RF reference using CORDIC and NCO. In SEL mode, the system can track the resonant frequency of the cavity within a certain bandwidth and in Open Loop mode, the system can synthesize drive signal of required amplitude and phase into the cavity using feed-forward tables. The open loop mode helps in system calibration and diagnostics.

An extensive data acquisition scheme has been developed and incorporated for monitoring and analysis. Implementation of data acquisition scheme is shown in Fig. 4. It can be divided into low speed and full speed data transfer. In low speed data transfer 1024 data points of 40 different waveforms can be displayed whereas in full speed data

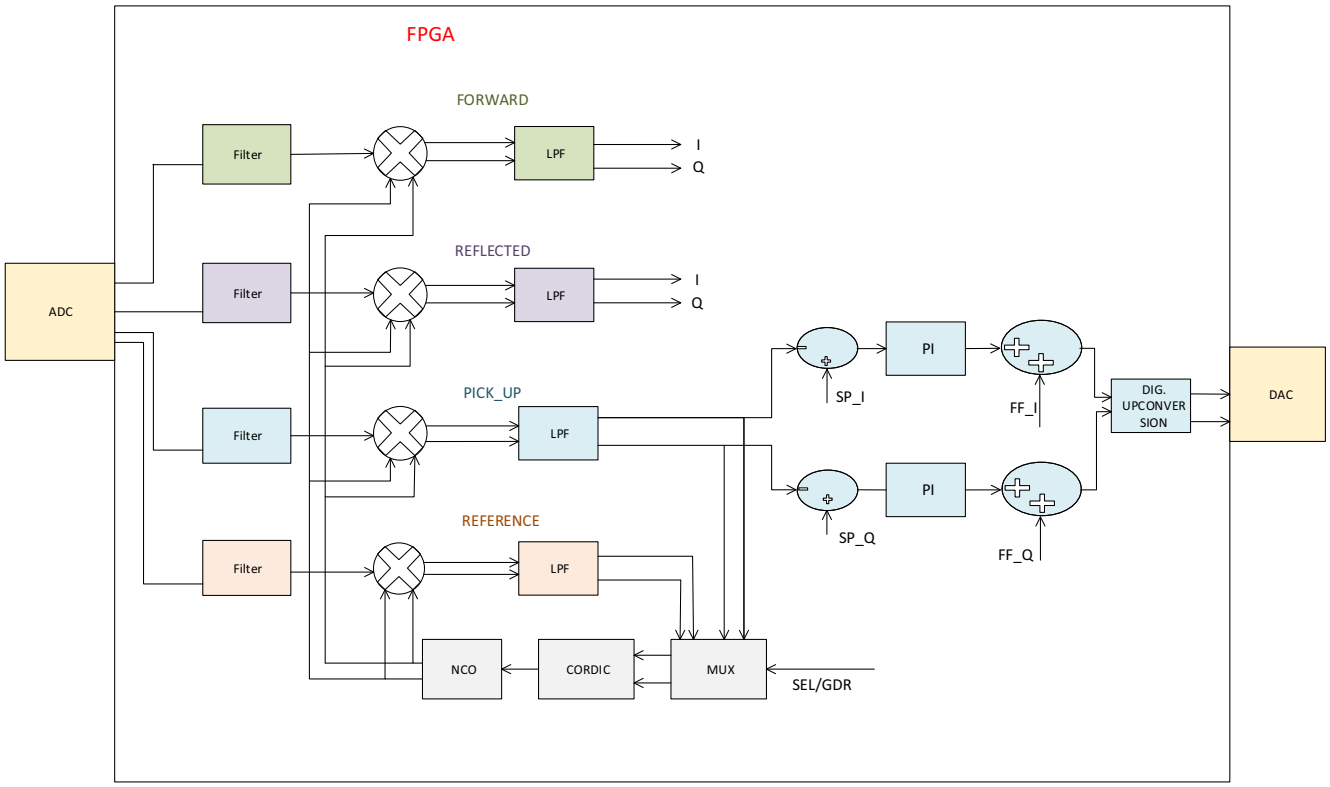


*Fig.3: Digital signal chain architecture.*

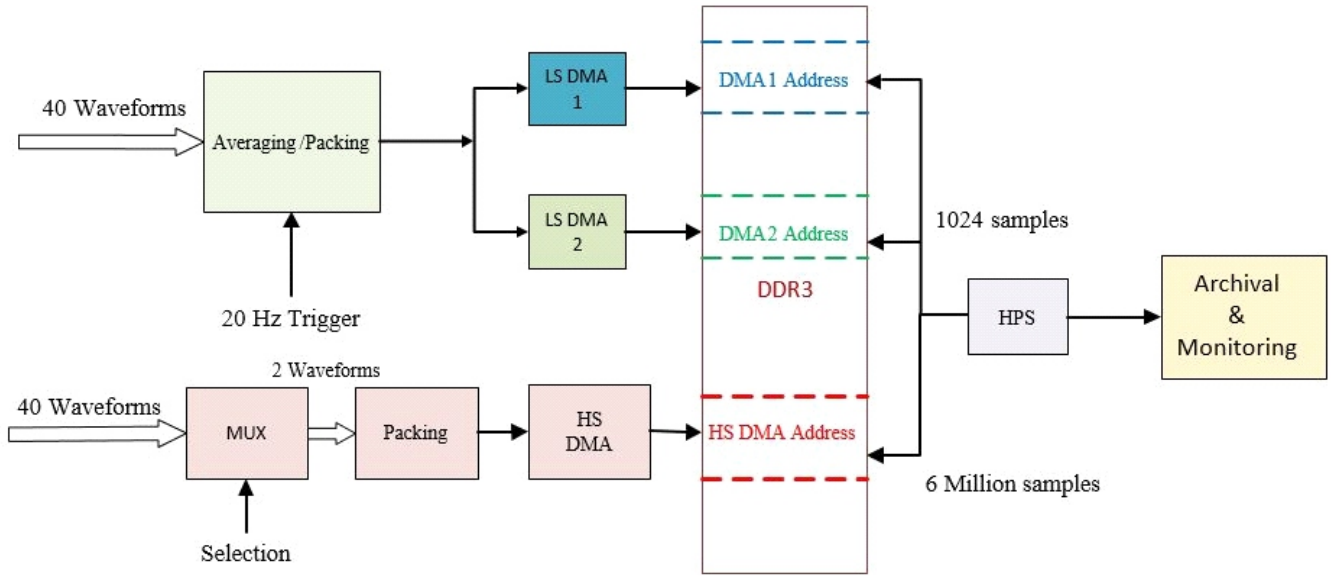


*Fig.4: Data acquisition and display implementation in FPGA.*

*Fig.5: RCS chassis.*

transfer any two of the 40 waveforms are acquired for duration of 64 ms. The high speed data transfer functionality helps in diagnostics and characterization.

### Resonance Control System

The Resonance Control System is a 19" rack mountable 3U size, standalone system, which is an independent operable sub-component of the integrated RF control system. Fig.5 shows the chassis of RCS with stepper motor driver, piezo drivers and digital board. Each RCS chassis supports tuning of four SCRF cavities. The system is interfaced to a host via Ethernet link and supports operation in manual as well as remote modes.

The system computes detuning of the cavity by using cavity base band equation. Excitation of Piezo actuator by half sine wave has also been implemented. Programmable half sine wave parameters, namely, width, amplitude, bias and delay with respect to RF pulse have been implemented in firmware and software.

### Control Software Description

The software platform consists of open source Preloader, U-boot, and Linux OS image and the Experimental Physics and Industrial Control System (EPIC)S SCADA [7]. Open source Preloader and U-boot have been configured in-house and cross-compiled using GNU bare-metal compiler for the SoC-FPGA platform. A custom configuration of the open-source embedded Linux is cross-compiled using GNU GCC compiler to prepare a bootable SD-card with the binaries of Preloader, U-boot, and OS image. EPICS IOC, responsible for LLRF system functionalities, is cross-compiled for ARM-based Linux OS and interacts with the FPGA using indigenously developed device drivers, loaded into the embedded Linux using customised device tree. EPICS IOC is then deployed on the HPC of the SoC-FPGA platform and interfaced with the FPGA.

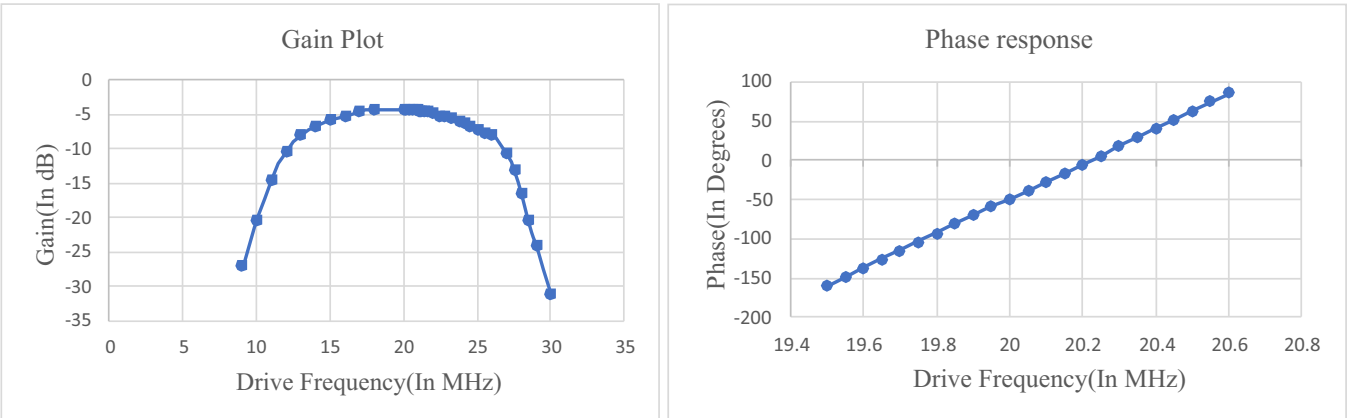


*Fig.6: Gain and Phase plot corresponding to different drive frequencies.*

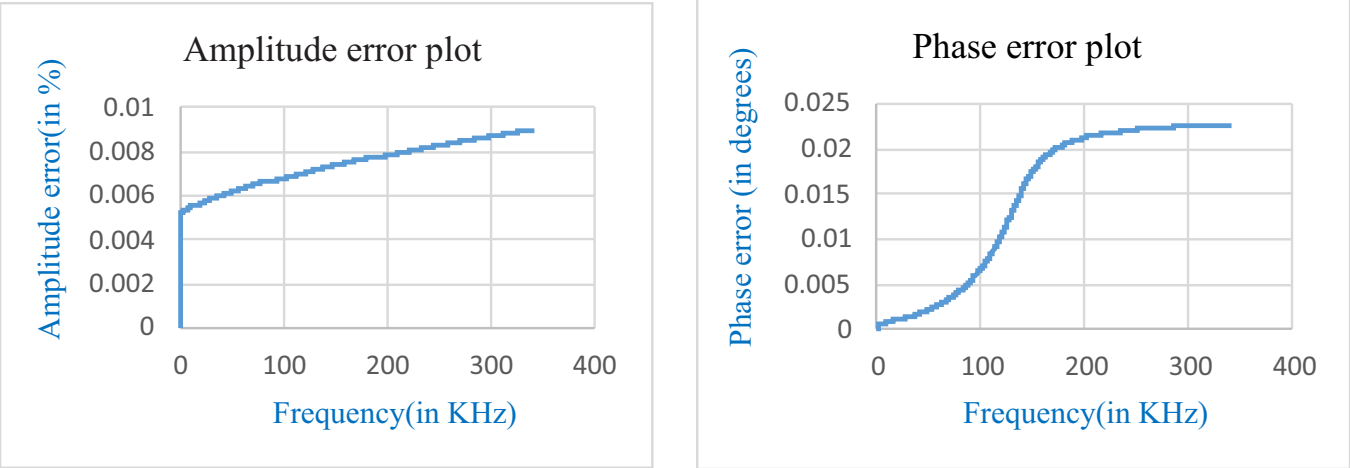


*Fig.7: Integrated Amplitude and Phase error w.r.t Frequency.*

*Table 1: Amplitude and phase measurement error w.r.t different ADC levels.*

| Sr. No. | Input level (percentage of ADC full range) | Amp error | Phase error (in degrees) |
|---|---|---|---|
| 1. | 25 % | 0.0106 % | 0.0237 |
| 2. | 32 % | 0.0094 % | 0.0233 |
| 3. | 62 % | 0.0082 % | 0.0228 |
| 4. | 78 % | 0.0077 % | 0.0230 |

### Testing in the Lab

The hardware and firmware have been thoroughly characterised through different tests in lab. In one of the tests, the digital module, up-converter and down-converter were connected to form a closed loop and drive signal was generated from feed forward tables in GDR mode. Phase and amplitude of the received signal in firmware were computed corresponding to different drive frequencies and results were used to estimate group delay and 3dB bandwidth of the system.

The gain and phase plot corresponding to different drive frequencies are shown in Fig. 6. The 3 dB bandwidth of the system is around 10 MHz and group delay was found to be 631.8 ns. The experiment was repeated after removing the up-converter filter and group delay in that case was found to be 541.9 ns with filter contributing around 90 ns of group delay.

In another experiment, capture and lock range of NCO phase loop was measured by driving the loop with different frequencies. Lock and capture range is a function of loop gain and for a typical loop attenuation value of 16, the Lock and capture range was found to be 340 kHz and 310 kHz respectively.

In order to achieve amplitude and phase stability of 0.01% and 0.01 degrees respectively, it is imperative that the noise in measurement of amplitude and phase should be much less than these values. In the test set up to estimate the intrinsic noise of the measurement chain, the required signals are generated through high quality signal generators locked to each other. The analog down-converter is fed with 650 MHz pick up and reference signals. The resulting IF signals are given to quad channel ADC and the phase and amplitude stability of the demodulated signal is calculated with firmware operating in GDR mode with feedback loop open.

The noise present in demodulated signal corresponding to pick-up has contributions from both amplitude dependent as well as independent sources, therefore, amplitude and phase stability has been calculated at various ADC input levels. The results are listed in Table 1. Integrated amplitude and phase fluctuations with frequency corresponding to an ADC input level of 32 % is shown in Fig. 7. As can be seen from Fig.7, measurement noise in closed loop bandwidth, which is of the order of few tens of kHz, is much less than the desired stability specifications.

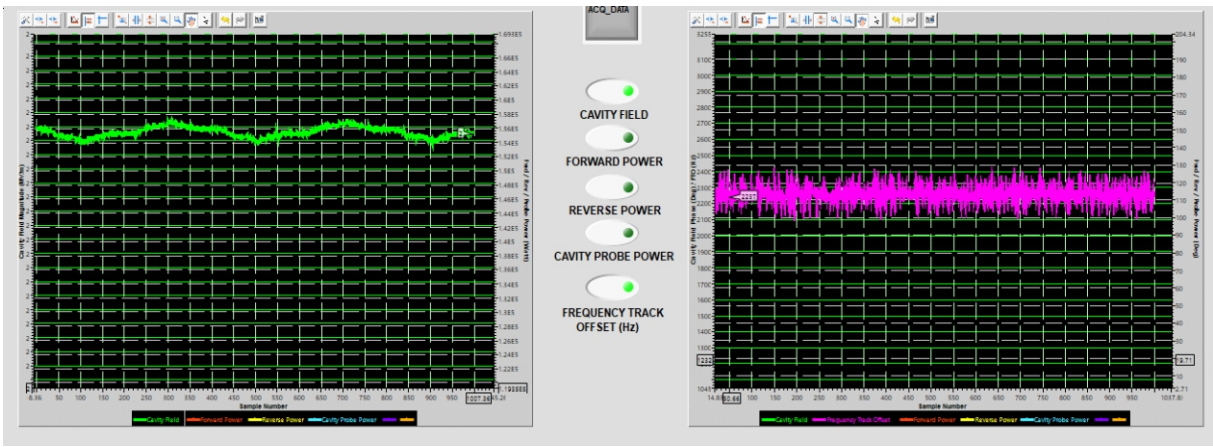


*Fig.9: SEL Mode of operation.*


*Fig.8: Integrated RF control system commissioned at HTS, RRCAT.*

### Commissioning at RRCAT

Subsequent to thorough testing in the lab at BARC, the integrated RF Control system, shown in Fig.8, was installed and commissioned at RRCAT for testing of 650MHz SCRF cavity in HTS. The cavity was tuned to the required resonance frequency with the use of tuning mechanism under stepper motor control. In SEL mode the cavity was tested up to 4.6 kW power. Fig.9 below shows field and detuned frequency of the cavity at 536 W power. The waveform in green represents RF field in the cavity. Even in the absence of amplitude feedback, the amplitude modulation is very small, highlighting the usefulness of SEL mode of operation. Adjoining plot in magenta represents offset of the cavity resonance frequency, which is observed to be 2200Hz from 650MHz.

The system was operated in pulsed mode at different power levels and duty cycles. Phase of the loop was adjusted to find the peak of pick-up signal. GUI screenshot corresponding to 3KW of output power and 30 percent duty cycle is shown in Fig.10. A zoomed view is displayed in Fig.11. As can be seen from Fig.10, cavity field (Green trace) gradually builds and then decays during pulse off time. Initially when the field is not present, the resonant frequency is higher and as the field builds up, resonant frequency decreases because of Lorentz force detuning. The cavity was also tested in generator driven resonator (GDR) mode. The cavity could be successfully driven in CW mode at 1 kW of power.

The RCS was integrated with the cavity tuner assembly already existing at RRCAT and the stepper motor was moved beginning with the cavity at resonance frequency of 650MHz. The new resonance frequency was measured with the help of LLRF control system in SEL mode. A linear response of stepper motor control was observed over the entire tuning range of up to 50 kHz. The piezo actuators were evaluated by measuring the resonance frequency of the cavity over a range of 0V and 100V, and the corresponding detuned frequency was observed to be 1 kHz.

Fig.12a shows the graph of stepper motor steps versus cavity detuning frequency and Fig. 12b shows the piezo voltage versus cavity detuning frequency.

At HTS the operation of the RFPI system along with LLRF system was observed. The RFPI system operated the RF switch at the output of the LLRF system as required and successfully protected various RF components whenever the reflected power exceeded the set limit. The response time of the system

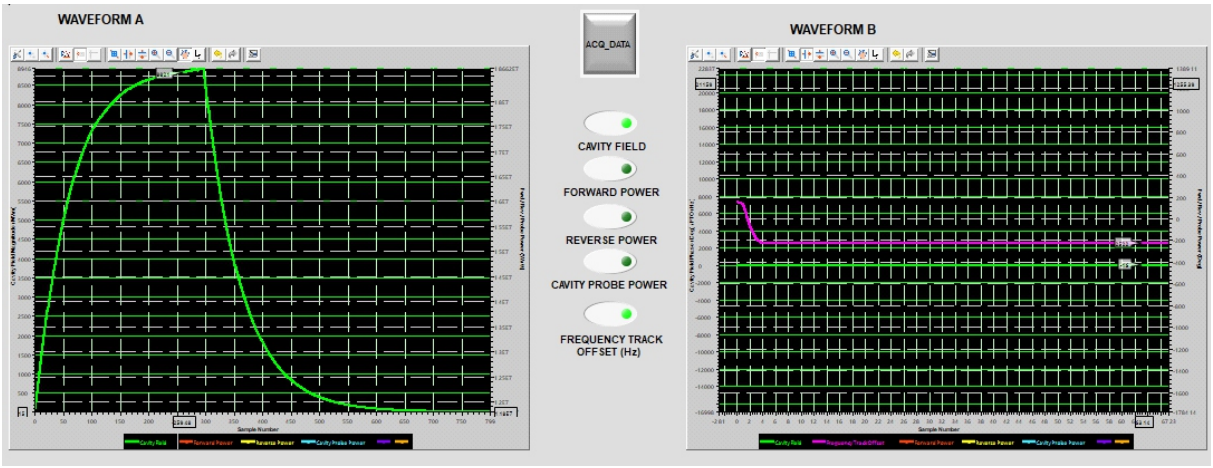


*Fig.10: SEL mode operation in pulsed mode.*


*Fig.11: Lorentz force detuning illustration in Pulsed mode.*

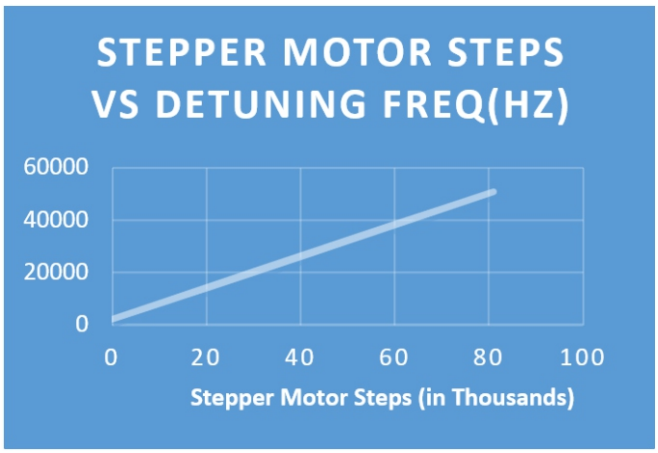


*Fig.12a: Performance of Stepper Motor at 2°K.*

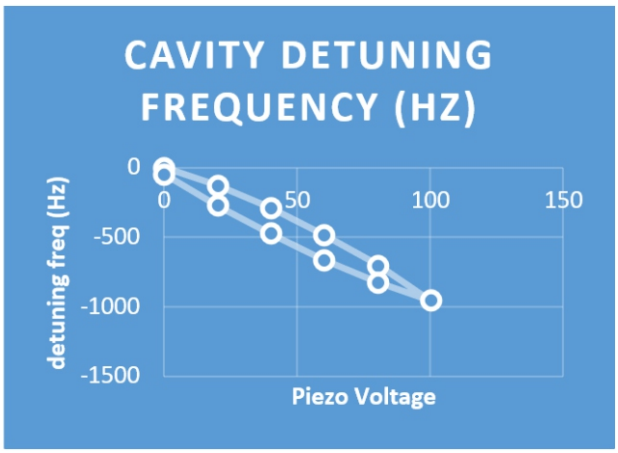


*Fig.12b: Performance of Piezo Tuner at 2°K.*

was within 1-2µs. Functionalities of RFPI system has been tested for long hours while characterising 650MHz, elliptical superconducting cavity. Different sub systems and signals interfaced to RFPI has been shown in Fig.13.

## Conclusion

Integrated RF control system consisting of LLRF system, RCS, and RFPI system. has been developed at ACnD, BARC under IIFC and commissioned at HTS, RRCAT for testing of 650 MHz superconducting RF cavities.

The LLRF system successfully established the RF fields in the cavity in SEL and GDR modes. It was observed that a few times, during conditioning phase of the cavity, RFPI switched OFF RF power to the cavity due to high reflected power and also due to fault status signal from MPS. The cavity was powered to 4.6 kW in the SEL mode and 1 kW in GDR mode without the need of automatic frequency tuning mechanism. The operation of HTS at RRCAT for the testing of 650 MHz RFSC gave an opportunity to validate the functioning of the RCS. The performance of the RCS with stepper motor controller was observed to be linear over the entire range. The plot above shows slight difference in the traces while raising and lowering the piezo voltage between 0 to 100V. The data acquisition system has aided in the operation and collection of data for analysis.

Based on the performance of the LLRF, RCS and RFPI systems in the HTS, an approval was received to deliver these systems to Fermilab for further testing. The systems have been shipped to Fermilab and await testing with the SCRF cavity.

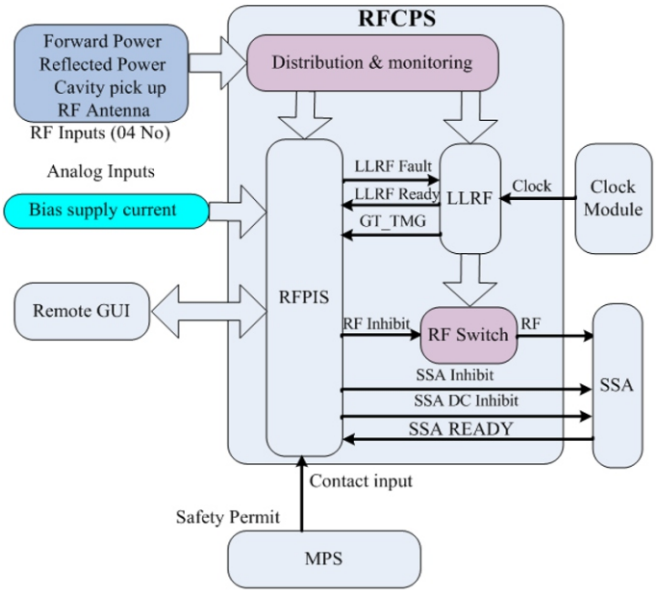


*Fig.13: Signals interfaced to RFPI at HTS, RRCAT.*

## Acknowledgment

We acknowledge the help and support of all the colleagues of ACnD during the entire development phase. The systems have been developed under IIFC and we sincerely acknowledge and appreciate technical support from the Fermilab during the design, fabrication and testing phases. The support of RRCAT team during the installation and commissioning of the systems was extremely valuable in all respects and is highly appreciated.

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