उच्च तीव्रता प्रोटॉन त्वरक

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निम्न ऊर्जा उच्च तीव्रता प्रोटॉन त्वरक (LEHIPA) के लिए निम्न–स्तर आरआफ नियंत्रण प्रणालियां

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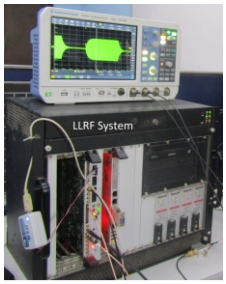

एल. एल. आर. एफ प्रणाली

सारांश

भाभा परमाणु अनुसंधान केंद्र,मुंबई के निम्न ऊर्जा उच्च-तीव्रता प्रोटॉन त्वरक (LEHIPA) के लिए एक डिजिटल निम्न स्तरीय रेडियो आवृत्ति नियंत्रण प्रणाली (LLRF) के स्वदेशी डिज़ाइन और कार्यान्वयन को प्रस्तुत किया गया है। निम्न स्तरीय रेडियो आवृत्ति नियंत्रण प्रणाली, आरएफक्यू, बंचर, डीटीएल1 और डीटीएल2 कैविटी में आरएफ क्षेत्र के आयाम और चरण पर सटीक नियंत्रण को सक्षम बनाती है। एडीसी, डीएसी, एफपीजीए, और क्लॉक संश्लेषक से सुसज्जित सीपीसीआई (cPCI) आधारित डिजिटल बोर्ड का लाभ उठाते हुए, प्रणाली आवश्यक सिग्नल प्रसंस्करण और नियंत्रण को लागू करती है। विलंबता को न्यूनतम करने के लिए फर्मवेयर को अनुकूलित किया गया है और इसमें प्रभावी एलएलआरएफ संचालन के लिए विविध प्रसंस्करण मॉड्यूल शामिल हैं।। एलएलआरएफ प्रणालियों की सफल तैनाती कई कैविटीज़ की समवर्ती लॉकिंग को सक्षम बनाती है, जिसके परिणामस्वरूप लेहिपा में 20MeV प्रोटॉन बीम की त्वरण प्राप्त होती है।

High Intensity Proton Accelerator

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Low Level RF Systems for LEHIPA

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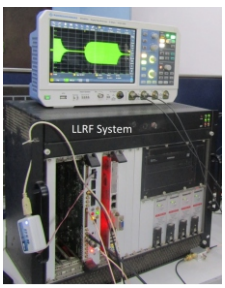

LLRF system

ABSTRACT

The indigenous design and implementation of a digital Low-Level RF (LLRF) control system for the Low Energy High-Intensity Proton Accelerator (LEHIPA) at BARC, Mumbai is presented. The LLRF system facilitates precise control over the amplitude and phase of RF field in RFQ, Buncher, DTL1 and DTL2 cavities. Leveraging a cPCI based digital board equipped with ADCs, DACs, FPGAs, and clock synthesizers, the system implements required signal processing and control. The firmware is optimized to minimize latency and includes diverse processing modules for effective LLRF operation. Successful commissioning of the LLRF systems enables simultaneous locking of multiple cavities, resulting in the attainment of 20MeV proton beam acceleration in LEHIPA.

KEYWORDS: *Accelerator, Buncher,* cPCI*, RF, Klystron, LEHIPA, Proton,* LLRF

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Introduction

A carefully and judiciously designed LLRF system based on digital techniques and incorporating FPGA offers unique advantages of precision, improved digital signal processing capabilities, possibility of implementing complex algorithms in FPGA, flexibility, programmability, repeatability and powerful diagnostic capabilities.

LLRF control system is one of the key subsystems in RF accelerator. Accelerator Control Division (ACnD), BARC has designed, developed and commissioned digital LLRF systems to control the amplitude and phase of RF field in resonant cavities in LEHIPA at BARC, Mumbai. LEHIPA consists of a 50keV ECR ion source, LEBT, 3MeV RFQ, Buncher cavity and Drift Tube Linac (DTL) section to deliver 20MeV proton beam. LEHIPA has a total of four LLRF systems for control of RF field in RFQ, Buncher, DTL1 and DTL2 as shown in Fig.1.

The LLRF system developed for LEHIPA is a compact cPCI based system, employing full digital approach, not requiring Up and Down converters. The hardware of the system consists of an Analog conditioning module (ACM) and a cPCI based digital board built around an FPGA. The ACM consists of input buffer/attenuation and the output drive amplifier sections. Pickup, Forward power and reflected power signals are digitized and processed. Windows based GUI application software has been developed for Control and display of parameters and data. The LLRF systems have been commissioned successfully for all the cavities of LEHIPA enabling extraction of 20 MeV proton beam. LLRF system has been modified for DTL so that it drives two RF Tanks (as shown in Fig.1) with single RF drive using Vector sum control method.

Hardware Description

Fig.2 shows the module level block diagram of the LLRF system. It consists of mainly two parts, namely,

a. Analog Conditioning Module (ACM), and

b. Digital Board.

RF signals from the field are received and conditioned by the ACM before feeding them to the digital board. High speed ADCs on the digital board digitizes the incoming RF signals and feeds the digital data to the FPGA for further processing. The LLRF system employs direct digitization scheme where it samples the incoming 352MHz RF signals directly without down-conversion. Feedback loop with PI controller is implemented in the FPGA for generating RF drive signal which after suitable amplification in the ACM, is fed to the Klystron through RF switch. The LLRF system supports pulsed and CW modes of operation. It is used in open loop mode during the RF cavity conditioning, and in closed loop mode during normal operation. Fig.3 is photograph of commissioned LLRF for RFQ at LEHIPA.

Analog conditioning module (ACM)

It is an FPGA based 19-inch rack mountable stand-alone module (Fig.4), remotely operated via Ethernet through Control System Studio (CSS) based application software. Analog signals are conditioned in this module to utilize the full dynamic range of the high speed multi-channel ADC's situated on the digital board. One ACM contains nine buffer channels and two

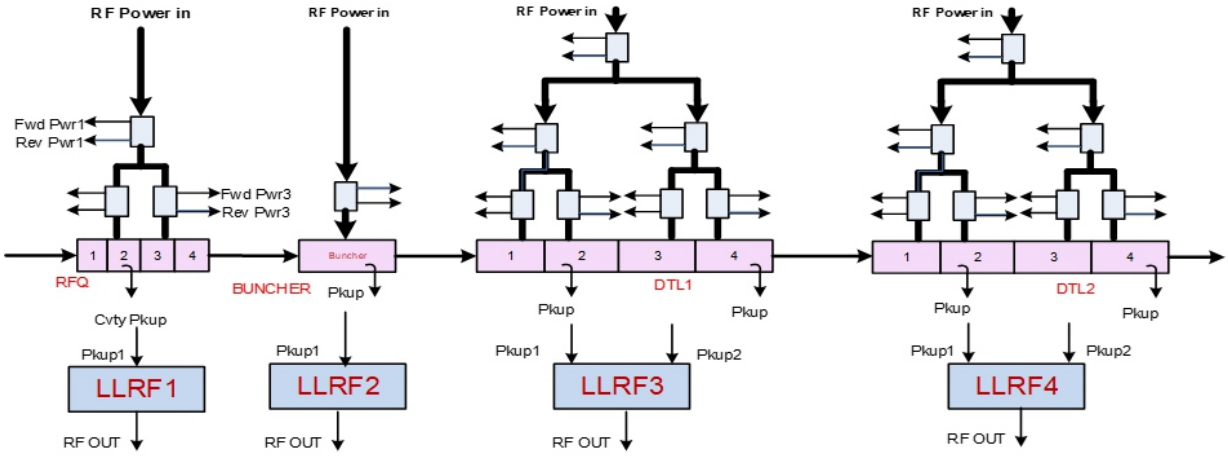

Fig.1: LLRF Systems for 20 MeV LEHIPA

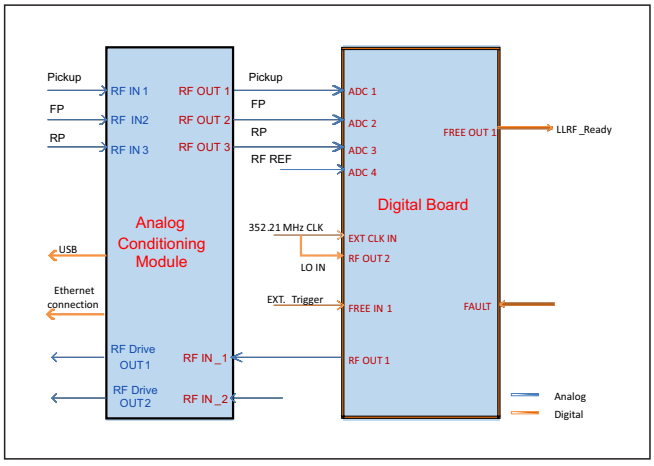

Fig.2: Modules in the LLRF System

Fig.3: LLRF system for RFQ, commissioned at LEHIPA

Fig.4:Analog conditioning Module

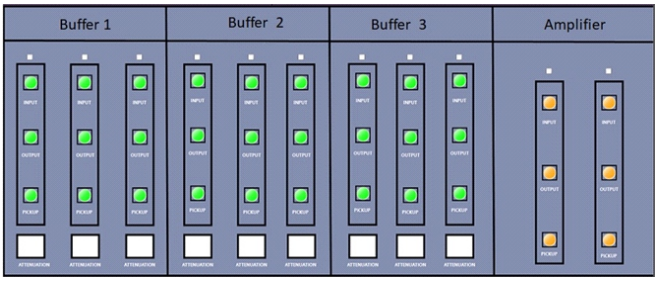

Fig.5: Analog Conditioning Module EPICS CSS GUI

amplifier channels and it can cater to two cavities. Buffer channel provides buffering and suitable programmable attenuation (0 to 15 dB) along with band-pass filtering to cavity RF signals. It protects Digital board from High levels of RF field signals. ACM also processes the RF drive out signal produced in the digital board. It buffers, filters and amplifies the drive out signal by 30db, which is further connected to the cavity via high power RF Amplifier. Fig.5 Shows the CSS GUI for ACM.

Fig.6: cPCI based Digital Board

Digital Board

The cPCI-based digital board, shown in Fig.6, includes an eight-channel ADC of suitable resolution for RF signal digitization, a high-density FPGA for data processing, and sufficient SRAM for storage, three low-speed DACs for tuner output and diagnostics, clock synthesizers for synchronized clock generation, and a dedicated cPCI controller for interface management. External 352 MHz RF signal, serves as the reference clock input. On board programmable clock synthesizers produce stable sampling clocks for ADCs and DACs. The digital board can simultaneously acquire and process eight analog signals, enabling control of two RF cavities. The firmware, optimized for minimal latency, includes

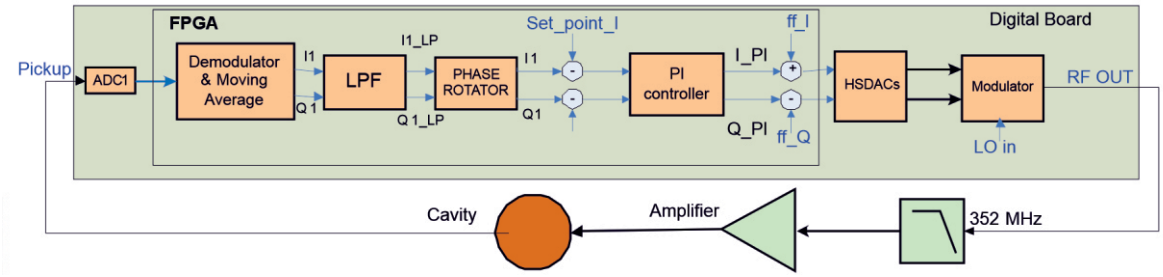

Fig.7: Implementation of feedback loop in digital board.

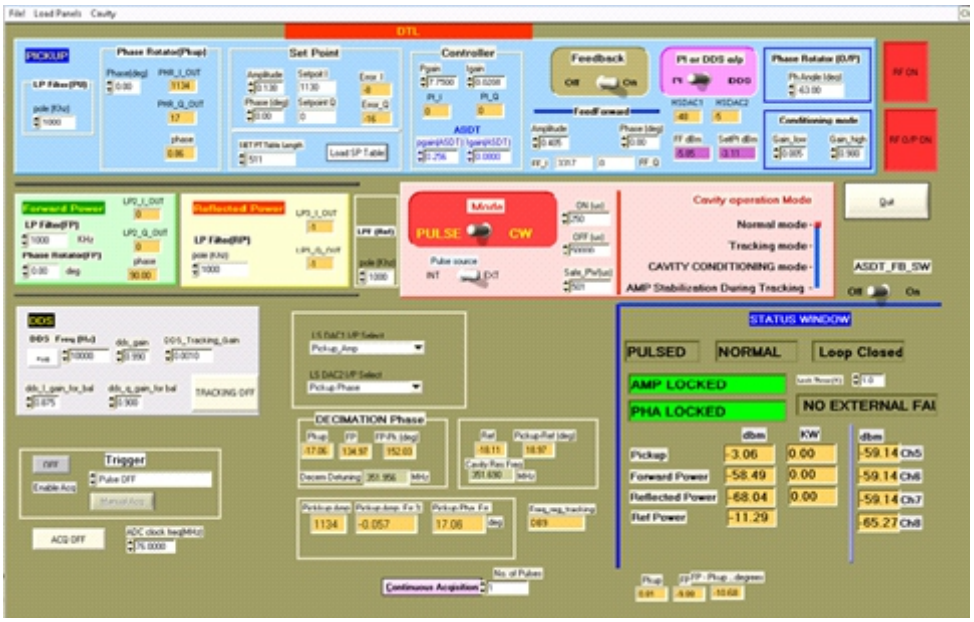

Fig.8: LLRF GUI in Amplitude and phase loop in lock condition for DTL.

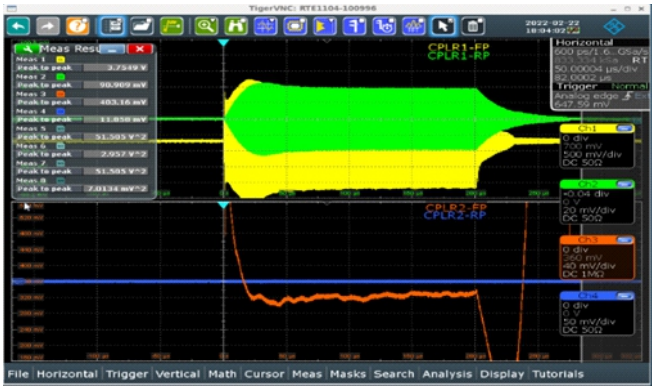

Fig.9: DTL forward power and pickup signals

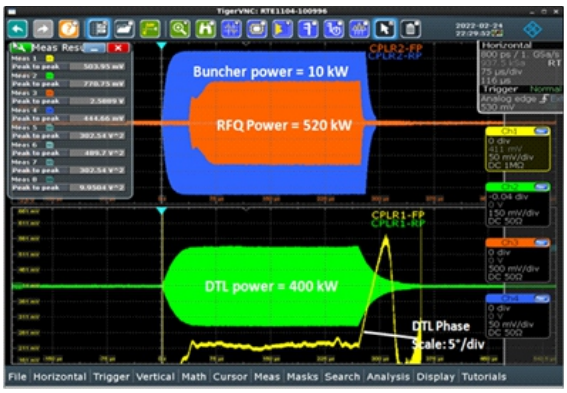

Fig.10: RFQ, Buncher and DTL1 locked at LEHIPA

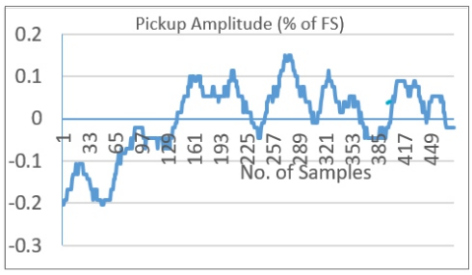

Fig.11: Pickup Amplitude for DTL1

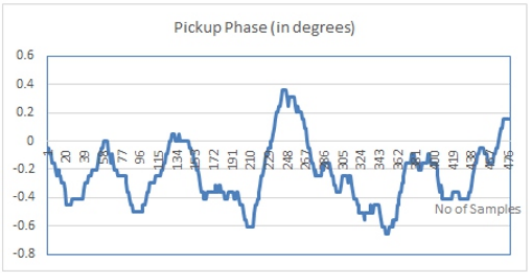

Fig.12: Pickup Phase for DTL1

various processing modules like quadrature demodulators, PI controllers, and data acquisition modules, ensuring smooth LLRF system functioning. The software facilitates communication with hardware for control diagnostics and data retrieval.

Feedback Control Loop

The pickup signal undergoes necessary signal conditioning and processing, as illustrated in the block diagram in Fig.7. The programmable gains in digital controller is useful in attaining optimal response for stabilizing the RF field within the cavity. Subsequently the on-board analog modulator generates the RF OUT which is conditioned and amplified by ACM for feeding to the klystron.

Software

The LLRF software controls all four LLRF systems at LEHIPA. Fig.8 shows main GUI of the system for DTL. It shows the amplitude and phase in DTL in locked condition.

Results

Fig.9 shows a screenshot of the oscilloscope, showing forward power and pickup signal for following conditions

DTL: 400kW Power, Pulse-Width =200us, Repetition rate=2Hz.

Fig.10 shows the pickup signals from RFQ, Buncher, and DTL1 under locked condition for 6.8 MeV operation. The yellow trace represents the phase of the DTL1 pickup, which falls within acceptable limits. Data for pickup amplitude (Fig.11) and phase (Fig. 12) for DTL1 has been acquired and amp and phase jitters have been found to be less than 0.2% and 0.2 degrees rms, respectively.

Acknowledgements

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